Listing of the Claims

1. (Previously Presented): Silicon-on-insulator comprising integrated circuitry, comprising:

a substrate comprising an insulator layer of silicon-on-insulator circuitry, the insulator layer comprising silicon dioxide;

a semiconductive silicon comprising layer of the silicon-on-insulator circuitry, the silicon comprising layer being received on the insulator layer, the silicon comprising layer comprising a pair of source/drain regions formed therein and a channel region formed therein which is received intermediate the source/drain regions;

a transistor gate received operably proximate the channel region; and

the insulator layer comprising a silicon nitride comprising region received intermediate the silicon dioxide comprising layer and the source/drain regions and running along only a portion of the channel region between the source/drain regions.

Claims 2 and 3 (Canceled).

4. (Previously Presented): The circuitry of claim 1 wherein the source/drain regions extend to the insulator layer.

Claim 5 (Canceled).

6. (Original): The circuitry of claim 1 wherein the silicon nitride comprising region has a thickness of from about 10 Angstroms to about 50 Angstroms.

7. (Previously Presented): Silicon-on-insulator comprising integrated circuitry, comprising:

a substrate comprising an insulator layer of silicon-on-insulator circuitry, the insulator layer comprising silicon dioxide;

a semiconductive silicon comprising layer of the silicon-on-insulator circuitry, the silicon comprising layer being received on the insulator layer, the silicon comprising layer comprising a pair of source/drain regions formed therein and extending to the insulator layer, the silicon comprising layer comprising a partially depleted channel region formed therein which is received intermediate the source/drain regions;

a transistor gate received operably proximate the channel region; and

the insulator layer comprising a silicon nitride comprising region received intermediate the silicon dioxide comprising layer and the source/drain regions and running along only a portion of the channel region between the source/drain regions.

Claims 8 and 9 (Canceled).

10. (Original): The circuitry of claim 7 wherein the silicon nitride comprising region has a thickness of from about 10 Angstroms to about 50 Angstroms.

Claims 11-61 (Canceled).

62. (Previously Presented): The circuitry of claim 1 wherein the silicon nitride comprising region contacts the silicon comprising layer.

63. (Previously Presented): The circuitry of claim 1 wherein the portion of the silicon nitride comprising region is discontinuous relative to the channel region.

64. (Previously Presented): The circuitry of claim 1 wherein the portion of the silicon nitride comprising region is continuous relative to the channel region.

65. (Previously Presented): The circuitry of claim 1 wherein the channel region comprises a central region laterally centered between the source/drain regions, the portion of the silicon nitride comprising region being laterally spaced from said central region.

66. (Previously Presented): The circuitry of claim 65 wherein the silicon nitride comprising region contacts the silicon comprising layer.

67. (Previously Presented): The circuitry of claim 1 wherein the channel region comprises a central region laterally centered between the source/drain regions, the portion of the silicon nitride comprising region running along said central region.

68. (Previously Presented): The circuitry of claim 67 wherein the silicon nitride comprising region contacts the silicon comprising layer.

69. (Previously Presented): The circuitry of claim 7 wherein the portion of the silicon nitride comprising region is discontinuous relative to the channel region.

70. (Previously Presented): The circuitry of claim 7 wherein the portion of the silicon nitride comprising region is continuous relative to the channel region.

71. (Previously Presented): The circuitry of claim 7 wherein the channel region comprises a central region laterally centered between the source/drain regions, the portion of the silicon nitride comprising region being laterally spaced from said central region.

72. (Previously Presented): The circuitry of claim 7 wherein the channel region comprises a central region laterally centered between the source/drain regions, the portion of the silicon nitride comprising region running along said central region.